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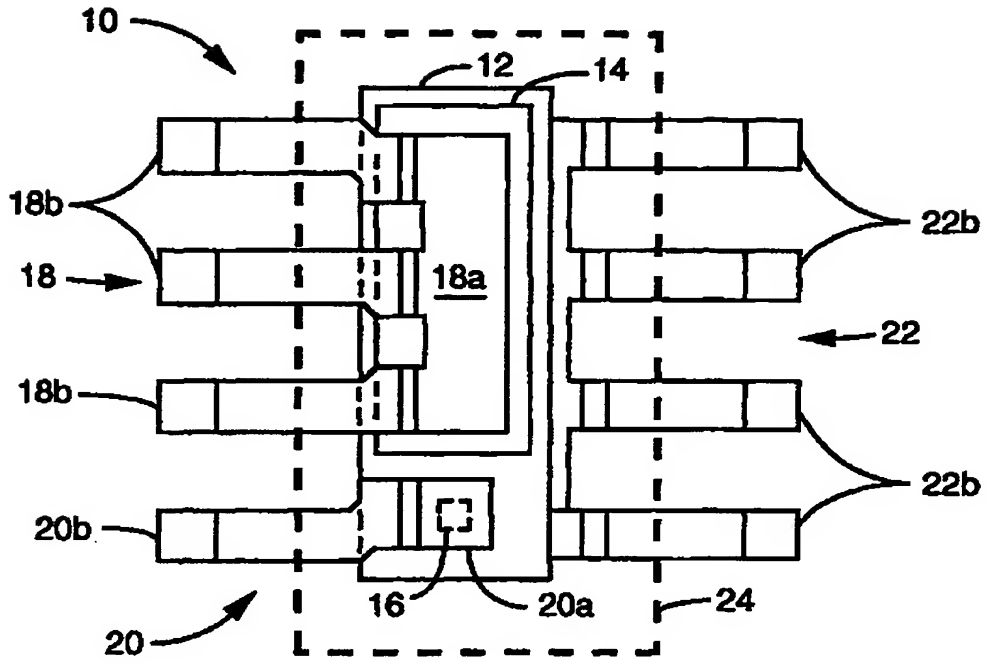
(54) IC chip package with directly connected leads

(57) An improved semiconductor device is disclosed. In one embodiment, the semiconductor device includes a semiconductor chip with contact areas on the top or bottom surface. A first lead assembly, formed from a semi-rigid sheet of conductive material, has a lead assembly contact attached to one of the contact areas of the semiconductor chip. The first lead assembly also has at least one lead connected to and extending from the lead assembly contact. A second lead assembly, also formed from a semi-rigid sheet of conductive material, has a lead assembly contact attached to another one of the contact areas of the semiconductor chip. The second lead assembly also has at least one lead connected to and extending from the lead assembly contact. An encapsulant encloses the semiconductor chip, the lead assembly contact of the first lead assembly and the lead assembly contact of the second lead assembly. The semiconductor device has low electrical and thermal resistance contributions from the package due to the direct connection of the lead assemblies to the chip. The semiconductor device may be formed as either a leaded package or a leadless chip carrier package.

EP 0 962 975 A2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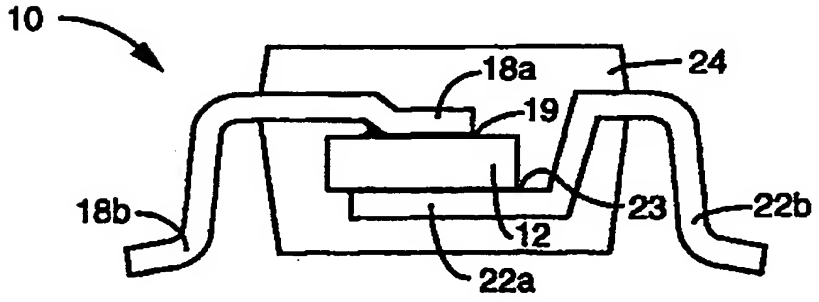
18b
18
18a
22b
22
18b
22b
20b
16
20a
24
20

FIG. 1A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18b
23
22b
12
22a

FIG. 1B

FIG. 2A

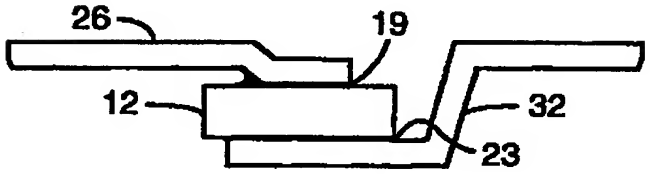


FIG. 2B

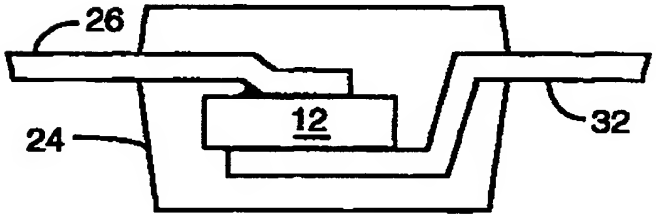


FIG. 2C

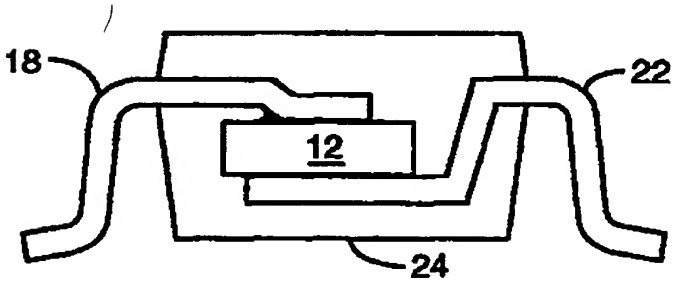
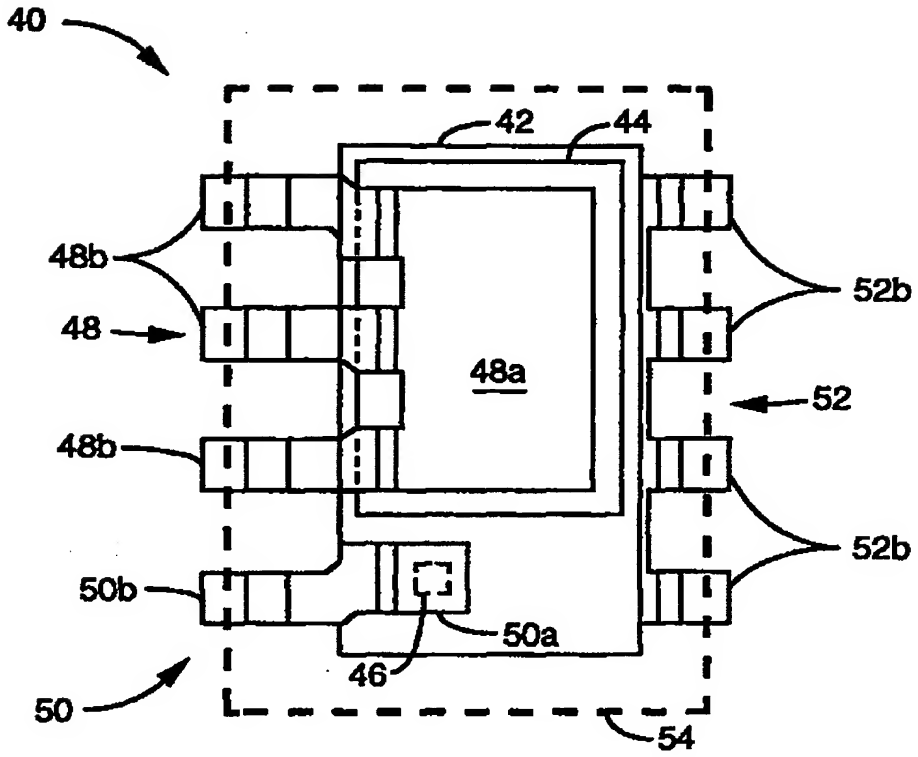


FIG. 2D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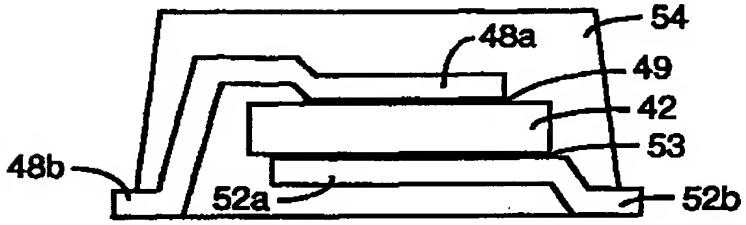
50b
50a
46
50
54

FIG. 3A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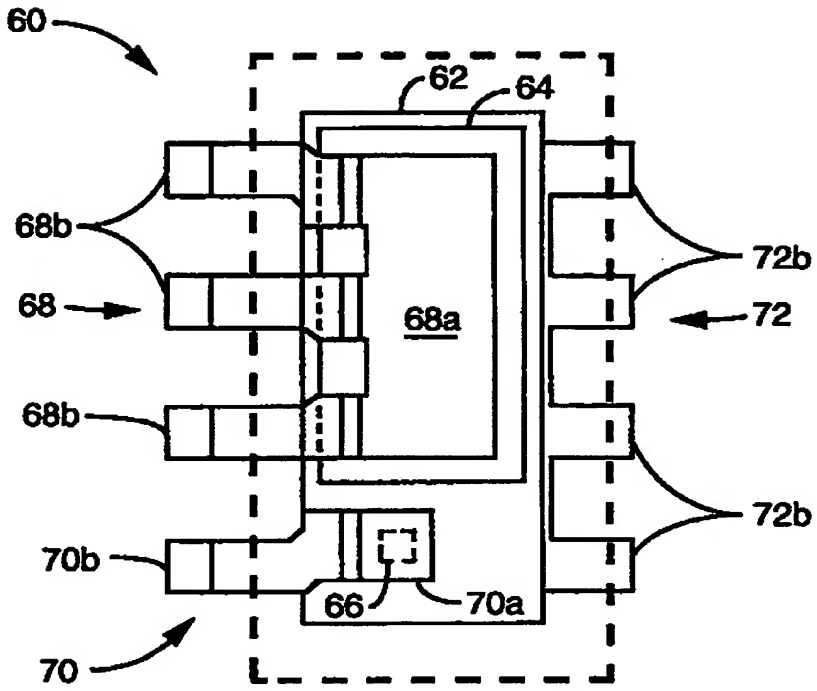
48a
49
42
53
48b
52a
52b

FIG. 3B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68a
72b
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68b
72b
70b
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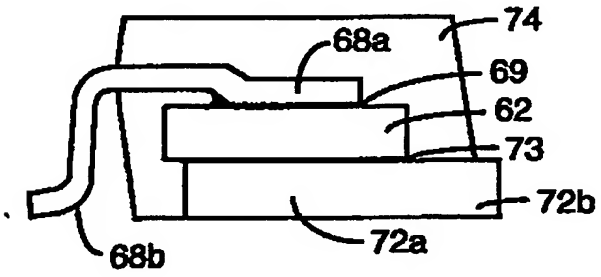
70a
70

FIG. 4A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68b

FIG. 4B

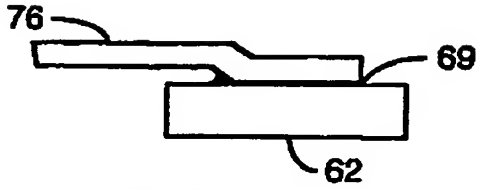


FIG. 5A

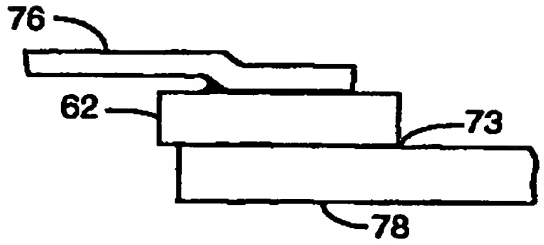


FIG. 5B

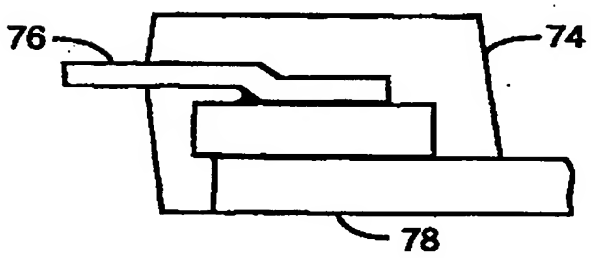


FIG. 5C

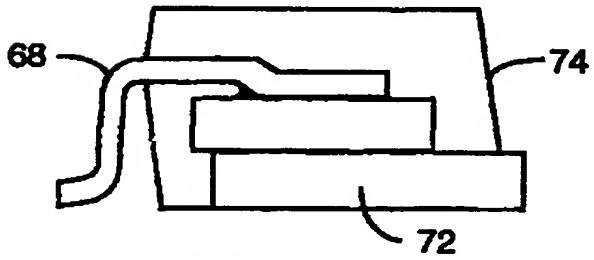
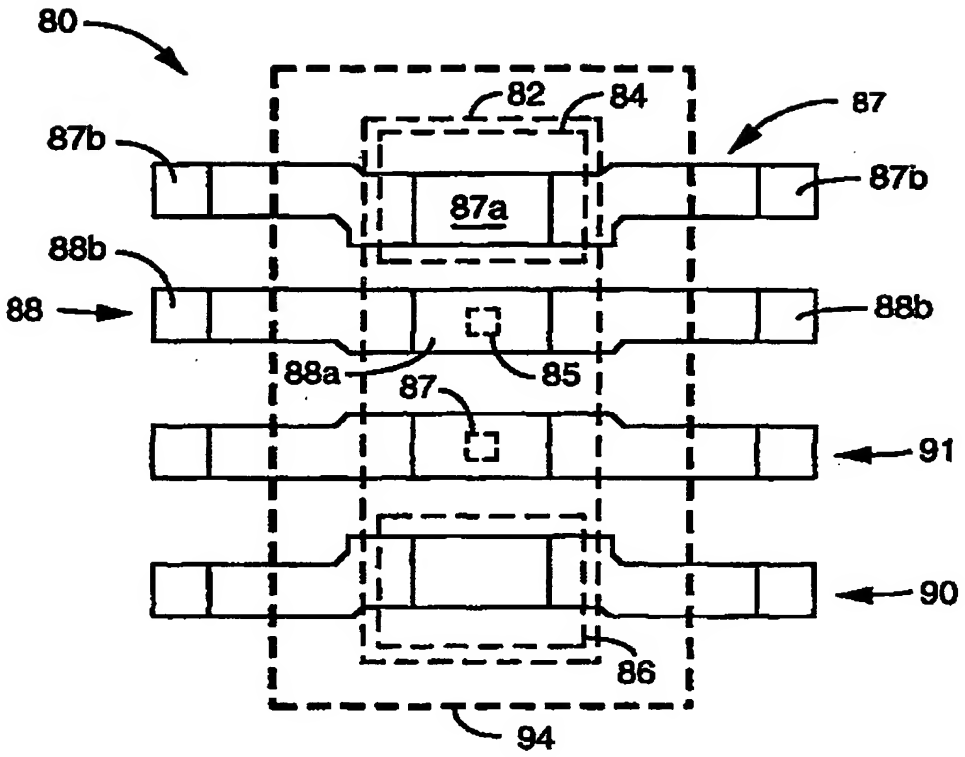


FIG. 5D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87b
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88b
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88b
88a
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86
94

FIG. 6A

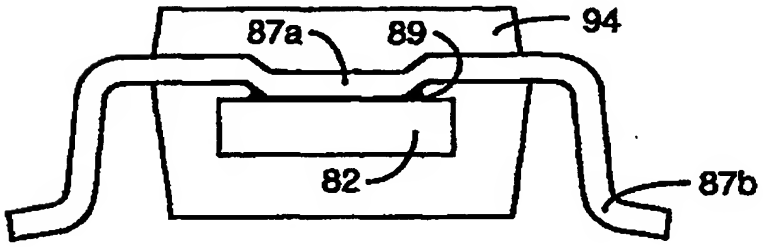
87a
89
94
82
87b

FIG. 6B

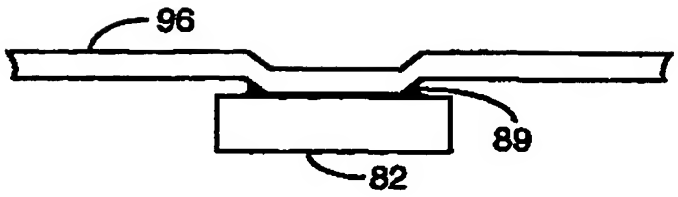

FIG. 7A

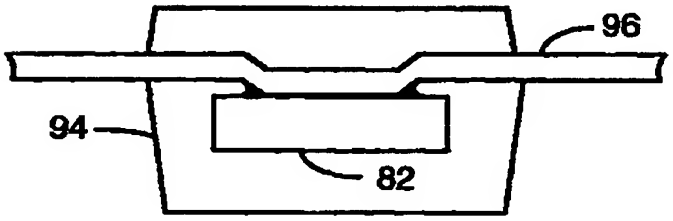

FIG. 7B

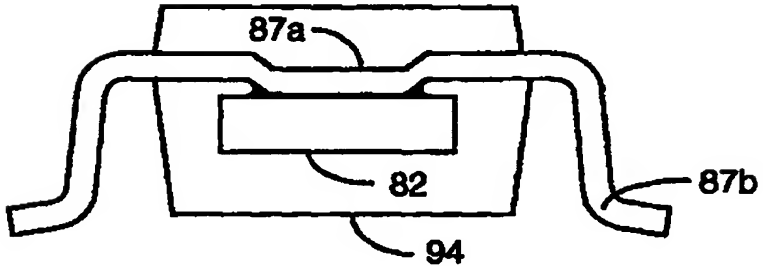

FIG. 7C

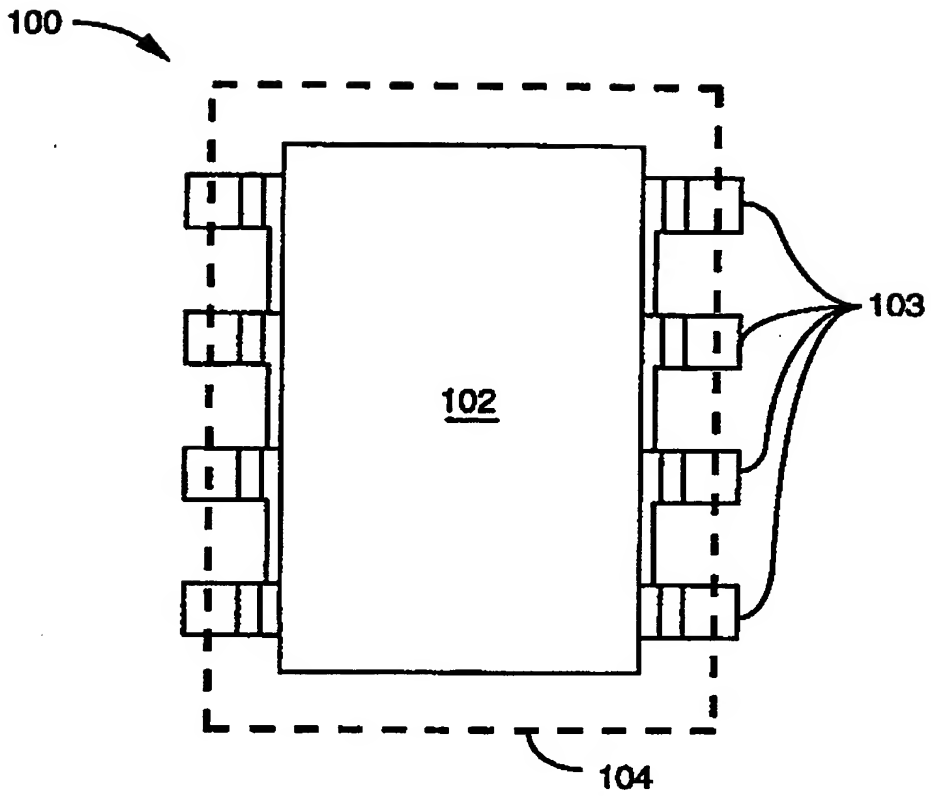

FIG. 8A

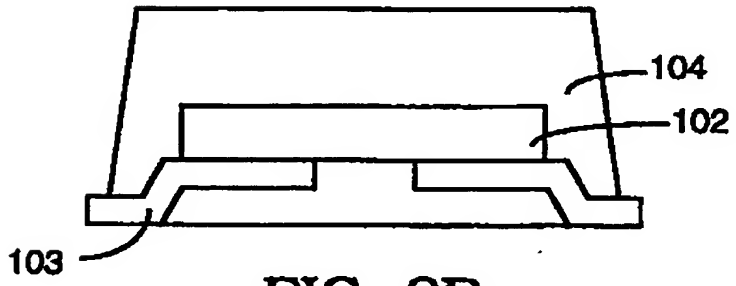

FIG. 8B